ABSTRACT OF THE DISCLOSURE

An encapsulated integrated circuit is provided including a semiconductor die, a printed circuit board, and an encapsulant. The printed circuit board is conductively coupled to the semiconductor die and comprises a laminate defining first and second major faces. The laminate includes a solder resist layer, an electrically conductive layer, and a bismaleimide triazine resin laminate including a selected laminated layer and an adjacent laminated layer. The electrically conductive layer is interposed between the solder resist layer and the underlying substrate. The selected laminated layer is disposed closer to the first major face than the adjacent laminated layer. The laminate includes at least one void formed therein so as to extend from one of the major faces through the solder resist layer and the electrically conductive layer at least as far as the adjacent laminated layer. The void is characterized by a varying profile that defines a ledge portion in the selected laminated layer and an underlying cavity in the adjacent laminated layer. The encapsulant is positioned to mechanically couple the semiconductor die to the printed circuit board and to extend through the void into the underlying cavity so as to form an adhesive bond with the bismaleimide triazine resin laminate. The semiconductor die is supported by the bismaleimide triazine resin laminate and the encapsulant and the bismaleimide triazine resin laminate are arranged to enclose substantially all of the semiconductor die.